

# CD5020 PWM Controller

## Features

- Internal High Voltage Start-Up Bias Regulator
- Error Amplifier
- High Precision Voltage Reference
- Programmable Soft-Start
- 1A Peak Gate Drive
- Maximum Duty Cycle Limiting — 80%
- Programmable Line Under Voltage Lockout (UVLO) with Adjustable Hysteresis
- Cycle-by-Cycle Over-Current Protection
- Slope Compensation
- Programmable Oscillator Frequency with Synchronization Capability
- Current Sense Leading Edge Blanking
- Thermal Shutdown Protection
- Packages: VSSOP10

## Applications

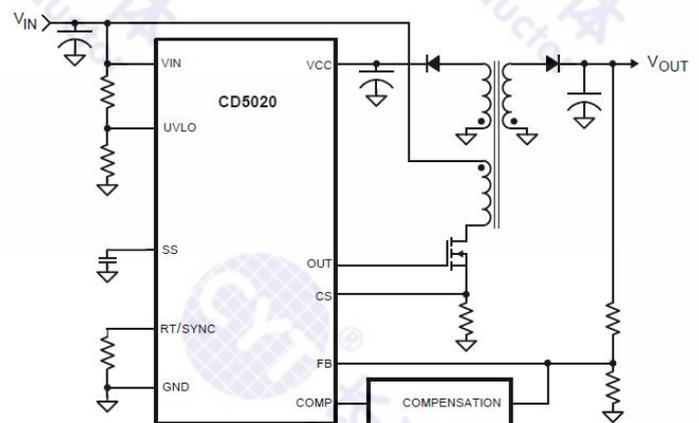
- DC–DC Power Supplies

## Description

The CD5020 high voltage pulse-width-modulation (PWM) controller contains all of the features needed to implement single ended primary power converter topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation.

The CD5020 includes a high-voltage start-up regulator that operates over a wide input range up to 100V. The PWM controller is designed for high speed capability including an oscillator frequency range to 1MHz and total propagation delays less than 100ns. Additional features include an error amplifier, precision reference, line under-voltage lockout, cycle-by-cycle current limit, slope compensation, soft-start, oscillator synchronization capability and thermal shutdown.

## Typical Application Circuit



## Pin Diagram (Top View)



## Absolute Maximum Ratings

$V_{IN}$ to GND	-0.3V ~ 100V
$V_{CC}$ to GND	-0.3V ~ 16V
RT to GND	-0.3V ~ 5.5V
All other PIN to GND	-0.3V ~ 7V

## Recommended Operating Conditions

$V_{IN}$ voltage	13V ~ 90V
External voltage applied to $V_{CC}$	8V ~ 15V
Operating junction temperature	-40°C ~ +125°C

## Electrical Characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
<b>Startup Regulator</b>						
$V_{CCReg}$	$V_{CC}$ Regulation	-	7.2	7.5	7.8	V
$I_{VCC-limit}$	$V_{CC}$ Current Limit	-	15	22	-	mA
$I_{VIN}$	Startup Regulator Leakage	$V_{IN}=36V$	-	270	500	$\mu A$
$I_{IN}$	Shutdown Current	$V_{UVLO}=0V, V_{CC}$ open	-	550	650	$\mu A$
<b>VCC Supply</b>						
$V_{VCC\_EN}$	$V_{CC}$ UVLO (Rising)	-	$V_{CCReg} - 300mV$	$V_{CCReg} - 500mV$	-	V
$V_{VCC\_DIS}$	$V_{CC}$ UVLO (Falling)	-	6.1	6.4	6.7	V
$I_{CC}$	Supply Current	$C_{LOAD}=0nF$	-	5	6	mA
<b>Error Amplifier</b>						
$GBW$	Gain Bandwidth	-	-	4	-	MHz
$A_{DC}$	DC Gain	-	-	75	-	dB
$V_{FB}$	Reference Voltage	$V_{FB}=COMP$	1.225	1.25	1.275	V
$I_{CPS}$	COMP Sink Capability	$V_{FB}=1.5V, COMP=1V$	5	10	-	mA
<b>UVLO Pin</b>						
$V_{UVLO}$	Shutdown Threshold	-	1.225	1.25	1.275	V
$I_{UVLO}$	Undervoltage Shutdown Hysteresis Current Source	-	36	40	44	$\mu A$
<b>Current Limit</b>						
$t_{LIM\_DLY}$	ILIM Delay to Output	CS step from 0V to 0.6V Time to onset of OUT Transition (90%)	-	30	-	ns
$V_{CS}$	Cycle by Cycle CS Threshold Voltage	-	0.45	0.50	0.55	V
$R_{SCS}$	CS Sink Impedance (clocked)	-	-	35	55	$\Omega$
$t_{LEB}$	Leading Edge Blanking Time	-	-	50	-	ns
<b>Soft-Start</b>						
$I_{SS}$	Soft-start Current Source	-	17	20	23	$\mu A$
$V_{SSC}$	Soft-start to COMP Offset	-	0.45	0.65	0.85	V
<b>Oscillator</b>						
$F_{OSC1}$	Frequency1	RT=31.6k $\Omega$	300	330	360	kHz
$F_{OSC2}$	Frequency2	RT=9.76k $\Omega$	930	1000	1070	kHz
$V_{SYNC}$	Sync threshold	-	2.4	3.2	3.8	V

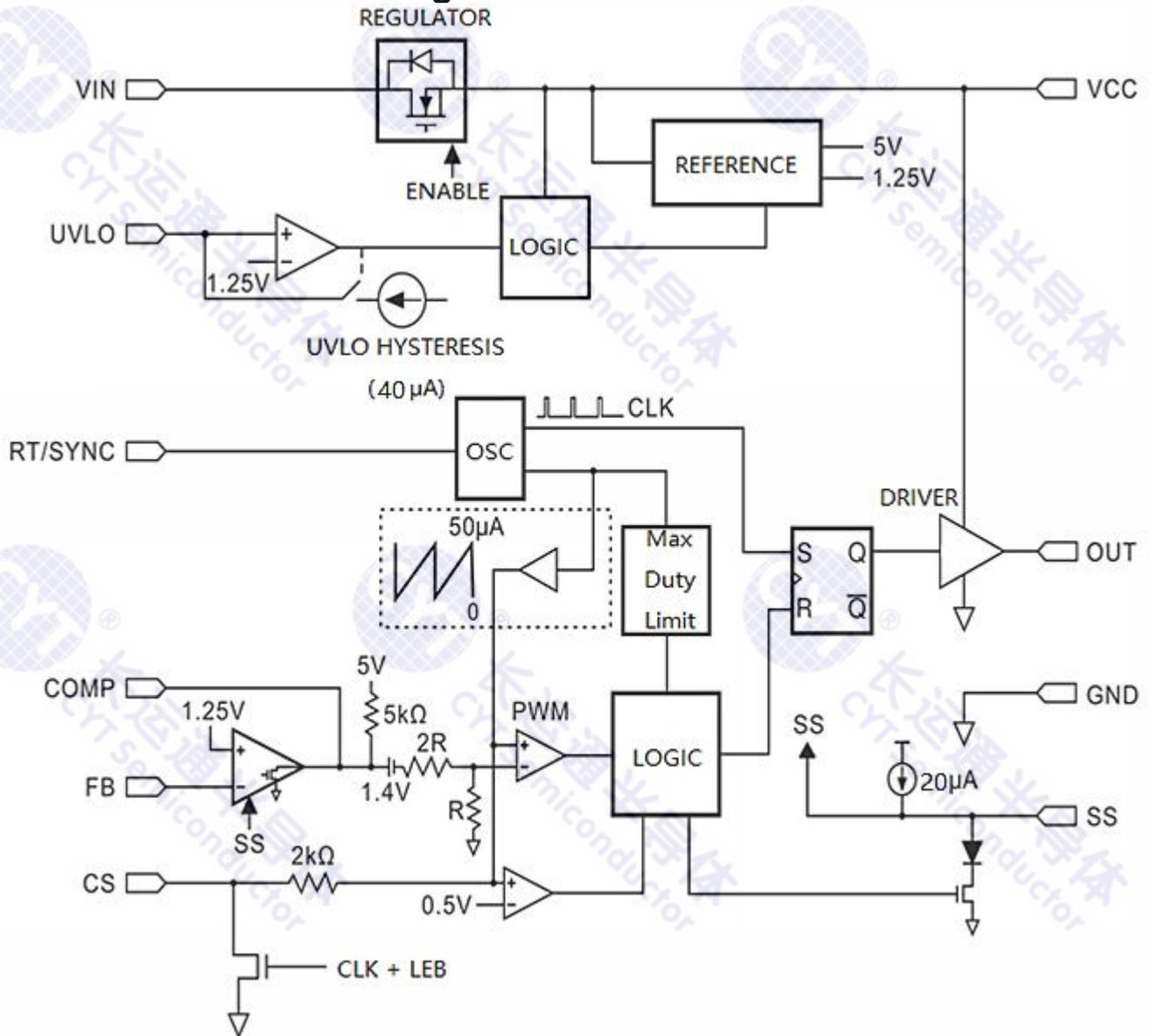
## Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
<b>PWM Comparator</b>						
$t_{OUT\_DLY}$	Delay to Output	COMP set to 2V, CS stepped 0V to 0.4V, Time to onset of OUT transition low	-	25	-	ns
$Duty_{(min)}$	Min Duty Cycle	$V_{COMP}=0V$	-	-	0	%
$Duty_{(max)}$	Max Duty Cycle	-	70	75	80	%
$A_{PWM}$	COMP to PWM Comparator Gain	-	-	0.33	-	V/V
$V_{COMP}$	COMP Open Circuit Voltage	-	4.3	5.0	6.1	V
$I_{COMP}$	COMP Short Circuit Current	$V_{COMP}=0V$	0.6	1.1	1.5	mA
<b>Slope Compensation</b>						
$V_{SLOPE}$	Slope Comp Amplitude	-	80	105	130	mV
<b>Output Section</b>						
$V_{sat-high}$	Output High Saturation	-	-	0.25	0.75	V
$V_{sat-low}$	Output Low Saturation	-	-	0.25	0.75	V
$t_r$	Rise Time	$C_{LOAD}=1nF$	-	18	-	ns
$t_f$	Fall Time	$C_{LOAD}=1nF$	-	15	-	ns
<b>Thermal Shutdown</b>						
$T_{SD}$	Thermal Shutdown Temp.	-	-	165	-	°C
$T_{SD\_HYS}$	Thermal Shutdown Hysteresis	-	-	25	-	°C
Note 1: Unless otherwise specified: test condition $T_A=-40^{\circ}C \sim 125^{\circ}C$ , $V_{IN}=48V$ , $V_{CC}=10V$ , $RT=31.6k\Omega$ . Note 2: The frequency is calculated as follows: $RT = \frac{1}{F_{SW} \times 96 \times 10^{-12}}$ (The unit is $\Omega$ for $RT$ , $F_{SW}$ is the switching frequency, the unit is Hz).						

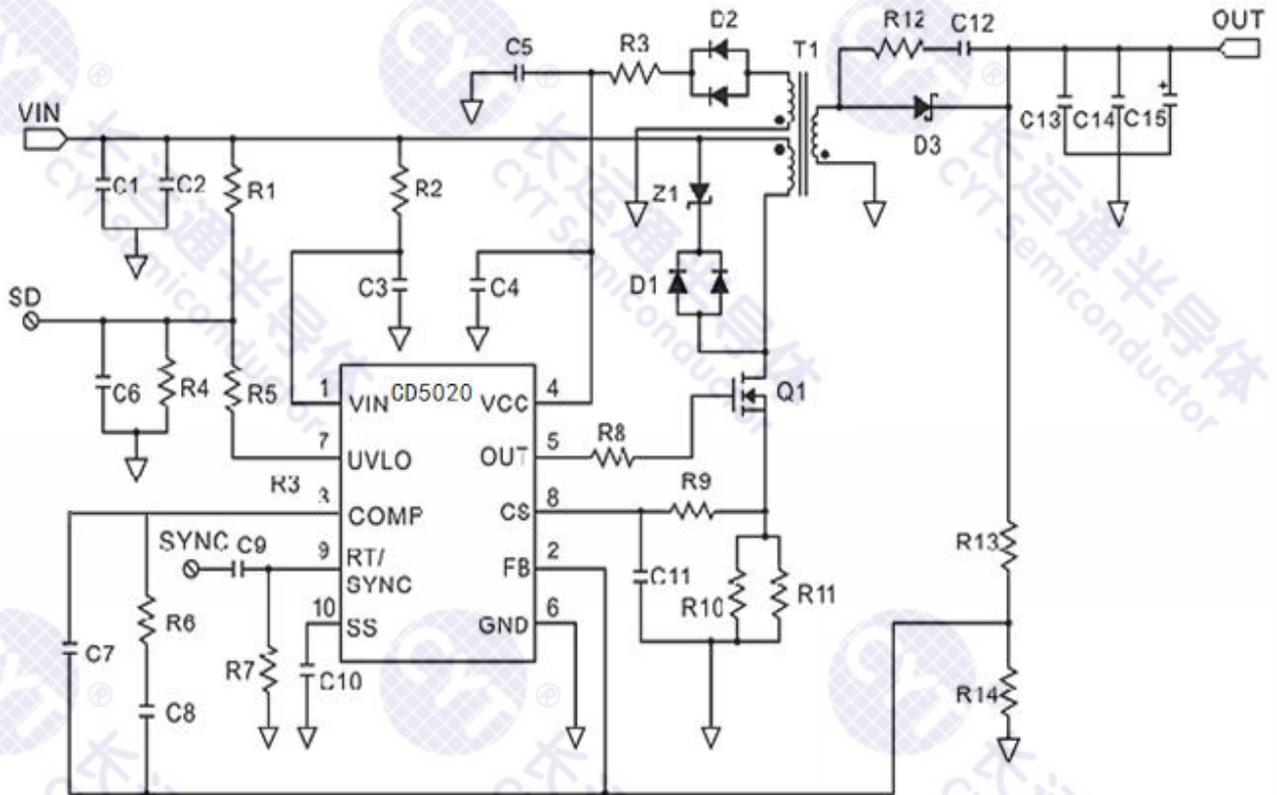
## Pin Functions

Pin	Name	Description	Application Information
1	VIN	Source Input Voltage	Input voltage range is 13V to 100V.
2	FB	Feedback Signal	Connecting to invert input of the internal error amplifier. The noninverting input is internally a 1.25V reference.
3	COMP	COMP Port	COMP pull-up is provided by an internal 5K resistor which may be used to bias an opto-coupler transistor.
4	VCC	Internal Supply Port	The voltage on this pin can be raised by the auxiliary winding to above the regulation set point, and the internal series regulator will shut down at this time to reduce this part of the power dissipation of the regulator.
5	OUT	Output Port	Output PWM control signal with a 1A peak current capability.
6	GND	Ground Return	The chip's electrical ground.
7	UVLO	Line Under-Voltage Shutdown	An external resistor divider from the power converter source voltage sets the shutdown levels. The design threshold of the UVLO pin is a resistance of 1.25V. Hysteresis is set by a switched internal 20 $\mu$ A current source.
8	CS	Current Sense Input	This pin is the input of the current sampling signal. Current sense input for current mode control and over-current protection. Current limiting is accomplished using a dedicated current sense comparator. Once the CS pin voltage exceeds 0.5V, the PWM output pin will be turned off immediately, the PWM pin switches low for cycle-by-cycle current limiting. When the PWM output pin is high, CS remains low for about 50ns to avoid current spikes.
9	RT/SYNC	Frequency and Synchronization Input	An external resistor connected from RT to GND sets the oscillator frequency. This pin also accepts synchronization pulses from an external clock.
10	SS	Soft-Start Input	An external capacitor set the output soft-start ramp rate.

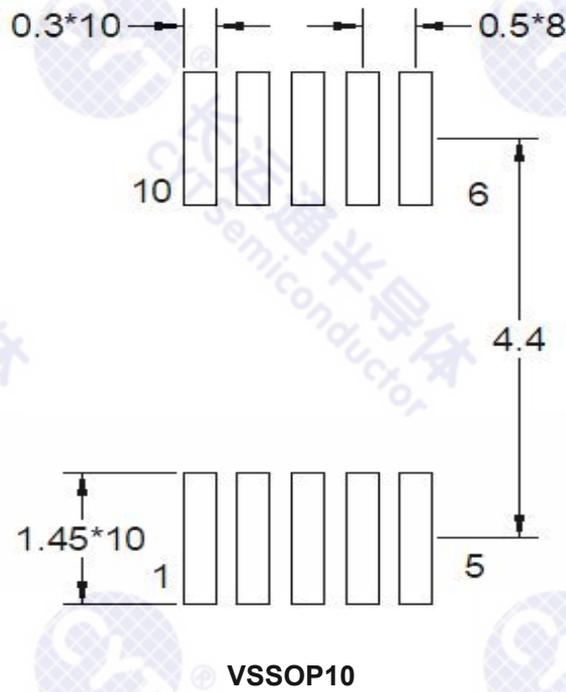
### Internal Function Block Diagram



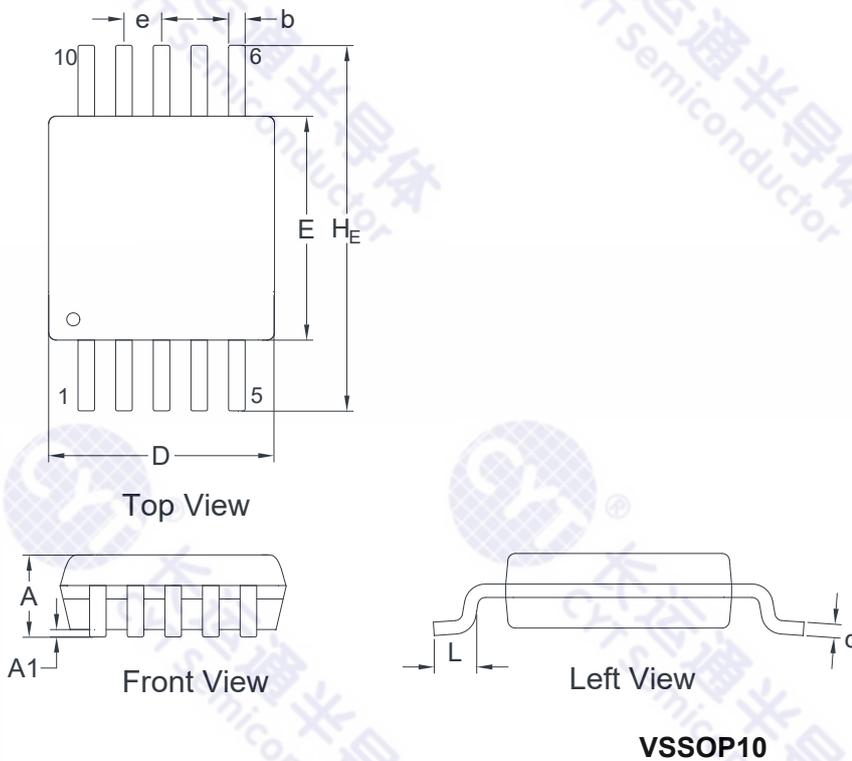
### Application Circuit



### PCB Layout Diagram



### Package Diagram



Size			
Symbol	Min	Max	Unit
A	--	1.10	mm
A1	0.0500	0.15	
b	0.1700	0.27	
c	0.13	0.23	
D <sup>a</sup>	2.90	3.10	
E <sup>a</sup>	2.90	3.10	
e	0.50		
H <sub>E</sub>	4.75	5.05	
L	0.45	0.75	
<sup>a</sup> The size does not include burrs.			

## Order Information

Model	Package
CD5020IVS	VSSOP10

## Declaration

1. The product cannot be used for equipment or devices that may cause personal injury or death for military, aircraft, automobile, medical, life support or life-saving. If you need to apply high reliability products to the above specific equipment or devices, please contact our sales staff to obtain relevant data manuals and samples.
2. Our company shall not be responsible for the quality of any of our products which are damaged by improper use or by exceeding even for a moment the rated value (such as maximum value, operating range, or other parameters) during use.
3. Our company continuously improves product quality, reliability, function or design, and reserves the right to change specifications.
4. Without the authorization of the company, the specification shall not be copied in whole or in part.